REMARKS

Claims 34-49 were renumbered by the Examiner as claims 21-36. Claims 1-20 have been canceled from the parent case. Claims 21, 26, and 29 have been amended.

Rejections of the Claims under 35 U.S.C. § 101

Claims 21-28 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Applicants respectfully request reconsideration of the rejection. Claims 21 and 26 are not directed to solely an abstract idea. Claim 21 specifically calls out the pausing of processing instructions at a pipeline stage for a period of time while processing at a pipeline stage. The operations described in claim 21 pertain to the processing of instructions at a pipeline stage of a processor. Accordingly, the operations are provided in a tangible environment and achieve the result stated in the preamble. Claim 26 includes similar limitations, and the same arguments apply. In view of the claim language to the physical environment for the performance of the method of claims 21 and 26, reconsideration and withdrawal of the rejection of claims 21-28 under 35 U.S.C. § 101 is respectfully requested.

Rejections of the Claims under 35 U.S.C. § 112, Second Paragraph

Claims 21- 25 and 29-36 were rejected under 35 U.S.C. § 112, second paragraph as failing to distinctly claim the present invention. As to claim 21, the Office Action objects to the claim as being unclear whether "the processing of instruction[s] will be paused when said first instruction is not of a first type." (emphasis in original). There is no requirement that a claim set forth such detail, only that the claim be distinct in its wording. Presumably, the claim is distinct as to if the instruction is of a first type. The focus of the claim is what operation to perform if that is the case, and thus, the claim is properly drafted. Similar arguments apply to claim 34,

which was similarly rejected.

Claim 21 was further rejected because the phrase "responsive to the determining operation" is allegedly not understandable. Though Applicants contend the claim language is distinct, the term "responsive to" has been changed to "in response to," which has the same meaning. As indicated in the claim, the resuming of processing of instructions of the first thread occurs in response to the determining operation set forth at lines 2-3 of the claim. That determining operation is to determine whether the first instruction if of a first type at a pipeline stage of a processor. An example of such an operation is described in the specification at pg. 5 with the pause instruction and its associated set and read microinstructions. The same arguments apply to claims 29 and 34.

As to claim 26, the Office action states that the claim omits essential elements. In particular, the Office Action states that the relationship between the determining step and the pausing step is missing. Claims 26 and 29 have been amended to indicate that the initialization of the counter is performed based on the determining operation. In view of the arguments and amendments above, reconsideration and withdrawal of the rejection of claims 21-25 and 29-36 under 35 U.S.C. § 112, second paragraph is respectfully requested.

Rejections of the Claims under 35 U.S.C. §§ 102(e) and 103(a)

Claims 21-25 and 29-33 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,493,741 to Emer et al. ("Emer"). Claims 26-28 and 34-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Emer.

In discussing the Emer reference, Applicants are making no admission that Emer has a filing date that predates the invention date of the present application.

In the Response to Arguments section, the Office Action provides new arguments as to the applicability of Emer to the pending claims. Applicants in their previous Amendment pointed out that in Emer, the entire thread processing unit is quiesced. If such a TPU includes

pipeline stages (though none are described in Emer), then none of those pipeline stages would be processing instructions from a second thread as called for in claims 21 and 26.

The Office Action points to Col. 5, lines 35-36 and Col. 7, lines 33-36 as describing pausing instruction of the first thread. The text at Col. 5 states that the QUIESCE instruction is "a request to quiesce, or halt, execution of the thread executing the QUIESCE." The text at Col. 7 indicates that when the QUIESCE instruction is executed, the TPU ceases executing instructions from the program. The Office Action further states that the Emer system includes a timer 107 as described at Col. 5, lines 63-64 and Col. 6, lines 9-11. As indicated by the text, the timer is started upon execution of the QUIESCE instruction.

The Office Action further points to Col. 4, lines 32-34 as allowing other executing programs to utilize available resources when the first thread is paused. The text of this section says "[h]alting execution of, or quiescing, the program results in a reduction of power consumption, and allows other executing programs to utilize available resources. The Office Action points to multiplexor 353 in Fig. 4 as providing a specific example of this. Claim 21 recites determining whether a first instruction for a first thread is an instruction of a first type at a pipeline stage of a processor and pausing processing of instructions of the first thread at said pipeline stage. As seen in Fig. 4, both of these operations are not being performed. There is no determination made at a pipeline stage that an instruction is of a first type and then pausing processing of instructions at said pipeline stage. In Emer, a QUIESCE instruction has been previously executed resulting in a quiesce state that is used for the Mapper operation shown in Fig. 4. Instructions after the QUIESCE instruction presumably were passed through multiplexor 353 before the QUIESCE instruction was executed. Accordingly, if a determination is made in Emer, it would be done at the execution unit of the processor, and other instructions already in the pipeline would continue to be processed. Claim 26, includes similar limitations to claim 21.

As to claims 29 and 34, these claims refer to a decode unit that is to determine whether a first instruction is of a first type and is to pause processing of instructions. In response to this

argument, the Office Action points to Emer's CPU including a decode unit and cites the language of Col. 5, lines 34-35, which describes the QUIESCE instruction as one that when executed halts execution of instructions in a thread. Applicants argument is that claims 29 and 34 refer to a decode unit having recited features, and that Emer does not teach or describe a decode unit having those features. The words "decode" or "decoder" do not appear in Emer. Even assuming that the CPU of Emer includes a decoder, since there is no mention of a decoder in Emer, it cannot be said that Emer teaches or suggest a decoder or decode unit that includes the features recited in the claims.

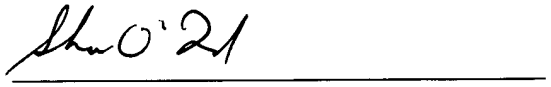
Since features of the claims are neither taught nor suggested by Emer, reconsideration and withdrawal of the rejection of claims 21-36 under 35 U.S.C. §§ 102(e) and 103(a) is respectfully requested.

CONCLUSION

The Examiner is invited to contact the undersigned at (202) 220-4255 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

Dated: 11/6/06

By: 

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